

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Docket No. 25740-02A

Feng-Tso Chien

Serial No.: To be assigned

Date Filed: Concurrently herewith

Title: Power Mosfet Device With Reduced Snap-Back and  
Being Capable of Increasing Avalanche-Breakdown  
Current Endurance, and Method of Manufacturing  
Same

Box Patent Application  
U.S. Patent and Trademark Office  
P.O. Box 2327  
Arlington, VA 22202

PRELIMINARY AMENDMENT

Prior to issuing a first office action, please amend the  
application as follows:

IN THE CLAIMS

Please add new claims 3-8 as follows:

3. (New) A power MOSFET device comprising:
  - an  $N^+$  silicon substrate;
  - a gate electrode;
  - an  $N^-$  epitaxial layer formed above said  $N^+$  silicon substrate, at least a portion of which is intermediate the  $N^+$  silicon substrate and the gate electrode;
  - a  $P^-$  well implanted in the  $N^-$  epitaxial layer;

a source contact region, etched into the  $P^-$  well, and formed of an  $N^+$  doped well and a  $P^+$  doped well, wherein the  $P^+$  doped well interfaces the  $N^-$  epitaxial layer and the  $P^-$  well, and the  $N^+$  doped well is spaced apart from and located above the  $P^+$  doped well;

whereby the snap-back is reduced and the avalanche-breakdown current endurance is increased.

4. (New) A method of manufacturing a power MOSFET device, comprising the steps of:

forming an  $N^-$  epitaxial layer on an  $N^+$  silicon substrate;

forming a gate layer above the  $N^-$  epitaxial layer;

implanting a  $P^-$  dopant to form a  $P^-$  well in the  $N^-$  epitaxial layer;

forming an  $N^+$  source region above the  $P^-$  well;

etching the  $N^+$  source region and implanting a  $P^+$  dopant to form a  $P^+$  well, wherein the  $P^+$  well interfaces the  $N^-$  epitaxial layer and the  $P^-$  well, and the  $N^+$  source region is spaced apart from and located above the  $P^+$  well;

depositing a glass layer; and

performing a metalization of the source contact and forming a drain contact;

whereby the snap-back is reduced and the avalanche-breakdown current endurance is increased.

5. (New) The method as claimed in claim 4, wherein the formation of the gate layer comprises the steps of:

etching a field oxide and growing a gate oxide layer;

depositing a polysilicon layer on the gate oxide layer, performing photomasking and etching the polysilicon layer.

6. (New) The method as claimed in claim 4, including the steps of applying a photomask of N<sup>+</sup> dopant and implanting N<sup>+</sup> dopant to form the N<sup>+</sup> source region above the P<sup>-</sup> well.

7. (New) The method as claimed in claim 4, including the steps of producing a photoresist prior to etching the N<sup>+</sup> source region and removing the photoresist after the P<sup>+</sup> well is formed.

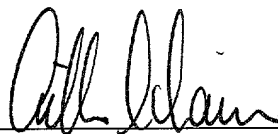
8. (New) The method as claimed in claim 4, wherein the glass layer is comprised of boro-phospho silicate glass.

REMARKS

This Preliminary Amendment is being filed concurrently with a new U.S. application. Consideration and allowance of the application, including newly presented claims 3-8, are respectfully requested.

Early and favorable action is earnestly requested.

Respectfully submitted,

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